REMARKS

Claims 1-20 were pending in the present application. Claims 1-20 have been cancelled. Claims 21-41 have been added. Accordingly, claims 21-41 are now pending.

The Examiner objected to Figure 1. Applicant has amended Figure 1 to include the phrase "Prior Art" (see attached replacement sheet). Applicant respectfully submits no new matter has been added.

The Examiner objected to the specification for various informalities. Applicant has amended the specification to overcome the objections. Applicant respectfully submits no new matter has been added.

The Examiner objected to claims 16, 18, and 19 because of informalities. Claims 16, 18, and 19 have been cancelled. Accordingly, Applicant believes the objection to now be moot.

Claims 10-14 stand rejected under 35 U.S.C. §112, 1st paragraph, as "failing to comply with the enablement requirement." Although Applicant respectfully disagrees with this rejection, claims 10-14 have been cancelled. Accordingly, Applicant believes the rejection to now be moot.

Claims 1-20 stand rejected under 35 U.S.C. §102(b) as being anticipated by de Corlieu et al. (U.S. Patent No. 4,891,810) (hereinafter "de Corlieu"). Applicant respectfully traverses portions of the rejections. However, in light of the foregoing claims amendments, Applicant believes the rejections to now be moot.

Rejection under 35 U.S.C. §112, 1st paragraph

In regard to the Examiner's assertion in the Office Action on page 4

> "Claim 10 claims a "method of manufacturing" the disclosed invention. Applicant fails to teach the method of manufacture of the "semiconductor device." The specification discloses that components of the invention are formed on a semiconductor device, however, there is no method included as to how this forming is accomplished."

Applicant discloses at page 4, lines 1-3 in the specification

> "A multiprocessor system chip 200 according to the present invention is shown in Figure 2. In this embodiment, eight processors 210-245 are formed on the die, and hence on the installed chip, and are connected to a crossbar circuit 270." (Emphasis added)

Accordingly, Applicant submits that any of a variety of well-known methods may be used to actually form the circuits in original claim 10.

Rejections under 35 U.S.C. 102(b)

Applicant's new claim 21 recites

A semiconductor device for use in a computing system, the semiconductor device comprising:

a plurality of processors formed on the semiconductor device;

a plurality of input/output (I/O) controllers formed on the semiconductor device and coupled to the plurality of processors such that **each** of the plurality of processors is coupled to **each** of the plurality of I/O controllers; and

a plurality of I/O interfaces formed on the semiconductor device and coupled to convey the data between the plurality of I/O controllers and the computing system;

wherein the plurality of I/O controllers are arranged to form a switching fabric including a plurality of communication

channels configured to convey data between **any** of the processors and **any** of the (I/O) interfaces;

wherein at least a portion of the processors and at least a portion of the I/O controllers are redundant." (Emphasis added)

de Corlieu is directed toward a reconfigurable computing device in which de Corlieu discloses in FIG. 1 a plurality of processors. However, in contrast to Applicant's claim 21, de Corlieu illustrates each of processors 100 being coupled to a respective receiving unit 480 for interfacing to one I/O bus. Specifically, de Corlieu teaches at col. 2 line 63 through col. 3 line 2

> "Advantageously, the processors 100 receive the data to be stored in the memory 3 through several wide-band buses 54. The use of several buses increases the transfer rates of the data transmitted.
> Advantageously, the computers according to the present invention comprise receiving circuits 480 which are used to transmit the data arriving at several buses 54 to **a single input/output bus 51 at the processor** 100. Since the bus 51 is small in length, its pass-band is, for example, equal to the sum of the total pass-band of the buses 54. In an alternative embodiment, its pass-band is smaller.
> Advantageously, the receiving circuits 480 can also be used for the electrical adaptation of the buses 54, thus increasing the transfer rate of the said buses.
> Advantageously, the receiving circuits 480 make it possible, through the use of a three-state electronic device for example, to insulate the processor 100 from the buses 54. This electrical insulation makes it possible, when all except one of the receiving circuits 480 are in high impedance, for the processor 100, which has its receiver circuit in low impedance, to transmit data to the bus 54. The receiver circuits 480 receives the operating commands partly from the direct memory access sequencer 504 through a bus 55. The other part of the commands comes directly from the associated processor 100 through the path 56." (Emphasis added)

From the foregoing, it is clear to the Applicant that de Corlieu does not teach, disclose, or fairly suggest "a plurality of input/output (I/O) controllers formed on the semiconductor device and coupled to the plurality of processors such that **each** of the plurality of processors is coupled to **each** of the plurality of I/O controllers;" nor does de Corlieu does not teach, disclose, or fairly suggest " a plurality of I/O interfaces formed on the semiconductor device and coupled to convey the data between the plurality of I/O

controllers and the computing system. In addition, de Corlieu does not teach, disclose, or fairly suggest "wherein the plurality of I/O controllers are arranged to form a switching fabric including a plurality of communication channels configured to convey data between **any** of the processors and **any** of the (I/O) interfaces," as recited in Applicant's claim 21.

Accordingly, Applicant submits that claim 21, along with its dependent claims, patentably distinguishes over de Corlieu for the reasons given above.

Applicant's claim 33 recites features that are similar to the features recited in claim 21. Thus, Applicant believes that claim 33, along with its dependent claims, patentably distinguishes over de Corlieu for at least the reasons given above.

CONCLUSION

Applicant submits the application is in condition for allowance, and an early notice to that effect is requested.

If any fees are due, the Commissioner is authorized to charge said fees to Meyertons, Hood, Kivlin, Kowert, & Goetzel, P.C. Deposit Account No. 501505/6000-00700/SJC.

Respectfully submitted,

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IN THE DRAWINGS:

Please find the attached Replacement Sheet which includes Figure 1. Applicant notes the only changes made to Figure 1 consist of adding the phrase "(Prior Art)" and removing the attorney docket and client docket designations from the upper right corner.